

PATENT APPLICATION  
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	Confirmation No. 8661
Tomoharu Tanaka et al.	)	Group Art No. 2824
Serial No.: 10/656,139	)	Examiner: LE, Vu Anh
Filed: September 8, 2003	)	Docket No: 001701.00676
For: Non-Volatile Semiconductor Memory Device	)	
Adapted To Store A Multi-Valued Data In A	)	
Single Memory Cell	)	

**INFORMATION DISCLOSURE STATEMENT**

**Mail Stop 313(c)**  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Attention: Karen Creasey  
Via Facsimile  
571-273-0025

Sir:

Pursuant to 37 C.F.R. §1.56 and in compliance with 37 C.F.R. §1.97, Applicants submit herewith Form PTO/SB/08, identifying information for consideration by the Examiner. A copy of the item of information is enclosed.

The undersigned certifies under 37 C.F.R. § 1.704(d) that each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counter part application and that this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this statement.

Applicants do not waive any rights to take appropriate action to establish patentability over the listed document should it be applied as a reference against the claims of the present application.

Consideration of the cited information and making the same of record in the prosecution of the above-noted application are respectfully requested. Should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: February 10, 2005

By: 

Joseph M. Potenza

Registration No. 28,175

1001 G Street, N.W.  
Washington, D.C. 20001-4597  
(202) 824-3000

Under the Paperwork Reduction Act of 1985, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Attorney Docket Number	001701.00676
------------------------	--------------

**If you need assistance in completing this form, call 1-800-PTO-9199 and select option 2.**

## Abstract (Basic): JP 9326199 A

The memory has a memory cell array (100) in which multiple non-volatile memory cells are configured. A bit-line is connected with the current flow path of the memory cell array and the word line is connected with the control gate of the cell array. Multiple sense latch circuits (110,120) and a bypass circuit (170) for the potential holder are connected with the bit-line of the memory cell array. Based on the predetermined data stored in the latch circuit, the data written-in the memory cell is checked for normal data write-in operation. When the threshold value of the data in the memory cell is less than the predetermined value, the potential of the bit-line from the bypass circuit is increased to high level by a voltage switching circuit (160). When the threshold value of the data is more than the predetermined value, then the potential value to the bit-line is released. ADVANTAGE - Enables data write-in operation control by threshold value adjustment. Shortens data write-in time in memory cell.

Dwg.2/21

Title Terms: ELECTRIC; ERASE; NON; VOLATILE; SEMICONDUCTOR; MEMORY; EEPROM; PORTABLE; TELEPHONE; PAGE; VOLTAGE; SWITCH; CIRCUIT; CONTROL; POTENTIAL; LEVEL; SUPPLY; BIT; LINE; CIRCUIT; BASED; THRESHOLD; VOLTAGE; LEVEL; DATA; WRITING; MEMORY; CELL

Derwent Class: U13; U14

International Patent Class (Main): G11C-016/02; G11C-016/06

File Segment: EPI

Manual Codes (EPI/S-X): U13-C04B2; U14-A03B7; U14-A07B

\*\*\*\*\*  
\*\*\* RX REPORT \*\*\*  
\*\*\*\*\*

RECEPTION OK

TX/RX NO	7997
RECIPIENT ADDRESS	202 824 3001
DESTINATION ID	
ST. TIME	02/10 17:42
TIME USE	06'31
PGS.	32
RESULT	OK